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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/711,503

09/22/2004

PEI-HAW TSAO

TSMC 2003-1622

5502

44045 7590 03/08/2007
BAKER & MCKENZIE
ON BEHALF OF TSMC
2300 TRAMMELL CROW CENTER
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DALLAS, TX 75201

EXAMINER

FARAHANI, DANA

ART UNIT

PAPER NUMBER

2891

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
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3 MONTHS

03/08/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

10/711,503

Applicant(s)

TSAO ET AL.

Examiner

Dana Farahani

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 11 December 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 16-26 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 16-26 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 16-18 and 20-26 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Koike et al. hereinafter Koike (US Patent Application Publication 2004/0036164), previously cited.

Regarding claims 16 and 26, Koike discloses in figure 10 a semiconductor package device, comprising:

a package substrate 2 having a first coefficient of thermal expansion and at least one bonding pad 6 on a surface of the package substrate; and

an integrated circuit chip 3 formed from a semiconductor wafer, the chip comprising: electrical devices formed therein (inherently in the chip),

at least one coupling structure 11 for bonding the chip to the at least one bonding pad on the package substrate; and

a final thickness less than a thickness of the semiconductor wafer (see paragraph 49), wherein the final thickness allows the chip to distort substantially with the package substrate during temperature changes despite the mismatch in their respective coefficients of thermal expansion (see also paragraph 65). A shape of the chip substantially conforms to a shape of the package substrate. See paragraph 74, wherein the chip and the substrate are cured together for

the purpose of curing the resin in between them. Since if the shape of the chip would have not substantially conform to the shape of the substrate during this temperature change, the chip would crack and become defective, it follows that the chip in fact conforms the shape of the substrate at least to some small degree, so the chip and a result the device would not become defective.

Although, Koike does not expressly disclose a second coefficient of thermal expansion different than the first coefficient of thermal expansion, it would have been obvious to one of ordinary skill in the art at the time of the invention to make the substrate from different material (i.e. different thermal expansion) than that of the chip for cost purposes.

Regarding claims 17 and 18, Koike discloses the claimed invention, as discussed above, except for the numerical amount of the thickness of the chip. It would have been obvious to one of ordinary skill in the art at the time of the invention to make the chip with a desired thickness in accordance to how much pressure the chip would be handling during and after the fabrication of the chip. See *In re Boesch*, 617 F. 2d 272, 205 USPQ 215 (CCPA 1980) for the proposition that discovering an optimum value of a result effective variable involves routine skill in the art.

Regarding claims 20-22, the coupling structure 11 is a lead free solder metal (Au); see paragraph 64.

Regarding claims 23 and 24, a dielectric encapsulant 12 is adjacent to a surface of the chip that is closest to the package substrate, and the one coupling structure is adjacent to the encapsulant.

Regarding claim 25, Koike discloses the claimed invention, as discussed above, except for the substrate is the material recited in the claim. It would have been obvious to one of

ordinary skill in the art at the time of the invention to select the material of the substrate from the materials recited in claim 25, in accordance to one of ordinary skill in the art preference of the material and cost considerations. See *In re Leshin*, 125 USPQ, for the proposition that it is within the general skill of a worker in the art to select a material on the basis of its suitability for an application. Note that substrate 2 has conductive traces therein (9 of figure 9).

3. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Koike as applied to claim 16 above, and further in view of Huang (US Patent 6,559,525), previously cited.

Koike discloses the claimed invention, as discussed above, except for a heat spreader coupled to the surface of the chip free of electrical devices.

Huang discloses in figure 7, heat sink 370 coupled to a surface of the chip 330. Therefore, It would have been obvious to one of ordinary skill in the art at the time of the invention to attach a heat sink to a surface of the chip of the Koike reference in order to dissipate heat which would be generated during the chip functioning.

Response to Arguments

4. Applicants' arguments filed 12/11/06 have been fully considered but they are not persuasive.

Applicants argue that the limitation of "a final thickness less than a thickness of the package substrate on which it is mounted, wherein the final thickness is selected so that the chip distorts substantially in accordance with distortion of the package substrate occurring during temperature changes such that a shape of the chip substantially conforms to a shape of the package substrate despite the mismatch in their respective coefficients of thermal expansion" is

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not discloses in the Koike reference. However, as discussed before, the final thickness of the chip is less than the thickness of the chip prior to the final stage (paragraph 65). Also, the chip and the substrate are cured together (see above). Since there is no evidence of cracking of the chip package, it follows that the device of the reference is defect free.

In regard to applicants' argument that any grinding done in the reference is for dimension consideration, while in the instant application it is done so a shape of the chip substantially conforms to a shape of the package substrate. However, choosing a certain thickness so that the chip substantially conforms to a shape of the package substrate is too broad, so that it could be said the end result of the thicknesses are to be considered. Clearly, the package of the reference goes through temperature changes, and therefore, the reference satisfies the functional requirement of claim 16, that of chip distorting in accordance with distortion of the package.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

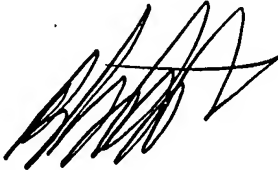
however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dana Farahani whose telephone number is (571)272-1706. The examiner can normally be reached on M-F 9:00AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571)272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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